THE CATHOLIC UNIVERSITY OF EASTERN AFRICA

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MAIN EXAMINATION

MAY – JULY 2019 TRIMESTER

FACULTY OF SCIENCE

DEPARTMENT OF COMPUTER AND LIBRARY SCIENCE

SPECIAL / SUPPLEMENTARY EXAMINATION

CMT 201: LOGIC CIRCUITS

Date: JULY 2019	**Duration: 2 Hours**
INSTRUCTIONS: Answer Question ONE and any other TWO Questions	

Q1 a) Simplify: $(A.B.(C+\overline{B.D})+\overline{A.B}).C.D$ **(4 marks)**

b) State the three notational methods for describing the behavior of gates and circuits **(3 marks)**

c) State the three representations of an XOR gate **(3 marks)**

d) Verify DeMorgan's law **(3 marks)**

e) Draw a circuit diagram corresponding to the following Boolean expression; $(\overline{BC})+\overline{(AB+\overline{C})}$ **(3 marks)**

f)

g) Consider the K-map shown in Figure 1.

00	01	11	10
0	0	1	0
1	1	0	1

Figure 1

State, in short hand notation, the

(i) Minterm **(3 marks)**

(ii) Maxterm **(3 marks)**

h) Convert

(i) decimal number 853 to Excess-3 **(1 mark)**

(ii) 7CH to its octal equivalent **(1 mark)**

(iii) decimal number 59.72 to its BCD **(1 mark)**

(iv) hexadecimal number 14B16to its binary equivalent **(1 mark)**

i) If $(10n01)_2 = (33)_r$. Find both *n* and *r*. **(4 marks)**

Q2 a) Consider the function: $Y = AB + (\overline{AC}).\overline{B}$

(i) Draw a combinational logic circuit that implements this function. **(3 marks)**

(ii) Draw a truth table for this function **(3 marks)**

(iii) Write a sum-of-products representation of Y **(2 marks)**

(iv) Write a product-of-sums representation of Y **(2 marks)**

b) A combinational circuit has 3 inputs A, B, C and output F.

F is true for following input combinations:

A is False, B is True.

A is False, C is True.

A, B, C are False.

A, B, C are True.

Use the convention True=1 and False = 0

(i) draw the Truth table for F **(4 marks)**

(ii) Write the simplified expression for F in SOP form using Karnaugh map. **(6 marks)**

Q3 a) Simplify the following Boolean expressions using a Karnaugh map. `

$(\boldsymbol{A},\boldsymbol{B},\boldsymbol{C},\boldsymbol{D}) = (\boldsymbol{C} + \mathrm{D}') + \boldsymbol{\overline{A}\,\overline{C}\,\overline{D}} + \boldsymbol{A\overline{B}\,\overline{C}} + \boldsymbol{\overline{A}\,\overline{B}\,C\,D} + \boldsymbol{A\,C\,D}$

(8 marks)

b) Using minterms, show that

$\overline{a}.c + \overline{b}.\overline{c} + a.b = \overline{a}.\overline{b} + b.c + a.\overline{c}$ **(5 marks)**

c) Design a combinational logic circuit that converts 4 bits binary to gray code **(7 marks)**

Q4 a) Determine the number of gates required to minimize the Boolean function Y= AB + CD using only 2 input NAND gates **(6 marks)**

b) Simplify the Boolean expression using Boolean laws hence verify using a truth table

$$f(w,x,y)=w\bar{x}y+wx+w\bar{y}+wx\bar{y}$$ **(7 marks)**

c) Design a combinational logic circuit (include block diagram and truth table) that performs arithmetic operation for adding three bits? **(7 marks)**

Q5 a) Draw a circuit that will satisfy the following conditions; A combinational feedback paths, one input x and one output z, 2 secondary variables y_1 and y_2 and 2 excitation variables Y1, Y2 such that the logic equations for the excitation variables in terms of the circuit input and secondary variables are

Y1 = $xy_1 + \bar{x}y_2$, Y2 = $x\bar{y}_1 + \bar{x}y_2$ and that Z = $\bar{Y}1.Y2$ **(10 marks).**

b) Design a combinational logic circuit that compares two, 2 bits binary numbers X and Y **(10 marks)**

END